E42 P54PCT SPB

CLAIMS

1. A method of arranging an on-chip capacitor creating a capacitance between a first conducting connection point in a first plane of the chip and a second conducting connection point in a second plane of the chip, **characterized in that** the method comprises creating at least one conducting extension of a first type from the first conducting point towards the second plane to a third plane, and creating at least one conducting extension of a second type from the second conducting connection point towards the first plane to a fourth plane, the fourth plane being located between the first plane and the second plane, and the third plane being located between the fourth plane and the second plane, and in that the first conducting extension is isolated from the second conducting extension by a dielectric allowing an electrical field to be created between the extensions.

2. The method according to claim 1, **characterized in that** the method further comprises creating a plurality conducting extensions of the first type.

3. The method according to claim 1 or 2, **characterized in that** the method further comprises creating a plurality of conducting extensions of the second type.

4. The method according to any one of claims 1 to 3, **characterized in that** the first plane is a side of a first metal layer, and the second plane is a side of a second metal layer, the first and the second metal layers being different metal layers.

5. The method according to claim 4, **characterized in that** the third and fourth planes are different sides of a third metal layer.

6. The method according to claim 4, **characterized in that** the third plane is a side of a third metal layer and the fourth plane is a side of a fourth metal layer, the third and the fourth metal layers being different metal layers.

7. The method according to any one of claims 1 to 6, **characterized in that** the method further comprises originating the conducting extension or extensions of the first type in a metal layer and terminating the conducting extension or extensions of the first type in a metal layer.

8. The method according to claim 7, **characterized in that** the method further comprises extending conducting extension or extensions of the first type through at least one further metal layer.

9. The method according to any one of claims 1 to 8, **characterized in that** the method further comprises originating the conducting extension or extensions of the second type in a metal layer and terminating the conducting extension or extensions of the second type in a metal layer.

10. The method according to claim 9, **characterized in that** the method further comprises extending the conducting extension or extensions of the second type through at least one further metal layer.

11. The method according to any one of claims 1 to 10, **characterized in that** the method further comprises extending the first conducting connection point in the first plane of the chip to comprise a conducting plate.

12. The method according to any one of claims 1 to 11, **characterized in that** the method further comprises extending the second conducting connection point in the second plane of the chip to comprise a conducting plate.

13. A method of creating an on-chip resonant circuit, **characterized in that** the method comprises arranging one or more capacitors according to any one

of claims 1 to 12, and at least one other passive component to thereby create the resonant circuit.

14. A method of creating an on-chip transmission line, **characterized in that** the method comprises arranging one or more capacitors according to any one of claims 1 to 12 in the transmission line.

15. An on-chip capacitor with a capacitance between a first conducting connection point in a first plane of the chip and a second conducting connection point in a second plane of the chip, **characterized in that** the on-chip capacitor comprises at least one conducting extension of a first type from the first conducting point towards the second plane to a third plane, and comprises at least one conducting extension of a second type from the second conducting connection point towards the first plane to a fourth plane, the fourth plane being located between the first plane and the second plane, and the third plane being located between the fourth plane and the second plane, and in that the first conducting extension is isolated from the second conducting extension by a dielectric allowing an electrical field to be created between the extensions.

16. The on-chip capacitor according to claim 15, **characterized in that** the on-chip capacitor further comprises a plurality conducting extensions of the first type.

17. The on-chip capacitor according to claim 15 or 16, **characterized in that** the on-chip capacitor further comprises a plurality of conducting extensions of the second type.

18. The on-chip capacitor according to any one of claims 15 to 17, **characterized in that** the first plane is a side of a first metal layer, and the second plane is a side of a second metal layer, the first and the second metal layers being different metal layers.

19. The on-chip capacitor according to claim 18, **characterized in that** the third and fourth planes are different sides of a third metal layer.

20. The on-chip capacitor according to claim 18, **characterized in that** the third plane is a side of a third metal layer and the fourth plane is a side of a fourth metal layer, the third and the fourth metal layers being different metal layers.

21. The on-chip capacitor according to any one of claims 15 to 20, **characterized in that** the conducting extension or extensions of the first type originates in a metal layer and terminates in a metal layer.

22. The on-chip capacitor according to claim 21, **characterized in that** the conducting extension or extensions of the first type extends through at least one further metal layer.

23. The on-chip capacitor according to any one of claims 15 to 22, **characterized in that** the conducting extension or extensions of the second type originates in a metal layer and terminates in a metal layer.

24. The on-chip capacitor according to claim 23, **characterized in that** the conducting extension or extensions of the second type extends through at least one further metal layer.

25. The on-chip capacitor according to any one of claims 15 to 24, **characterized in that** the first conducting connection point in the first plane of the chip comprises a conducting plate.

26. The on-chip capacitor according to any one of claims 15 to 24, **characterized in that** the second conducting connection point in the second plane of the chip comprises a conducting plate.

27. An on-chip resonant circuit, **characterized in that** the resonant circuit comprises one or more capacitors according to any one of claims 15 to 26.

28. An on-chip transmission line, **characterized in that** the transmission line comprises one or more capacitors according to any one of claims 15 to 26.

29. A transmission line based component such as a resonator, matching network, or power splitter, **characterized in that** the transmission line based component comprises a transmission line according to claim 28.